ESD Protection Structure Qualification – A New Approach
For System Level Reliability In Automotive Power Applications

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Abstract

ESD (electrostatic discharge) protection devices as part of the device pad circuitry of semiconductors are designed for a specific wafer technology and ESD withstanding voltage. These devices are protecting semiconductor products against damages due to electrostatic discharges. After successful qualification they will be released for a usage in high volume products where they must ensure the ESD robustness over the complete product lifetime.

All present automotive qualification standards e.g. AEC (automotive electronic council) or JEDEC do not cover the assessment of the typical drifts of the characteristic electrical ESD protection device parameters after application of device specific reliability stress tests under consideration of the target ESD stress [1-3].

The paper introduces a new methodology to characterize ESD protection diodes after ageing by BTS (bias temperature stress) reliability tests. The used devices are partly ESD pre-stressed before application of the reliability test. The influence of the reliability stress on the ESD robustness is evaluated by using an ESD post-stress.

The experimental results are presented. For ESD protection devices release targets for automotive power applications are defined. Due to the device ageing possible impacts for the final system level ESD robustness are concluded.

Kurzzusammenfassung


Sämtliche bestehenden Automotive-Qualifikationsstandards wie z.B. AEC (automotive electronic council) oder JEDEC decken die Bewertung der typischen elektrischen Parameterdriften dieser ESD-Schutzelemente nach durchgeführt chem Bauteilspezifischen Zuverlässigkeitstress unter Berücksichtigung des ESD-Stresslevels nicht ab [1-3].

Das Paper stellt eine neue Methodik für die Bewertung von ESD-Schutzdioden vor, die durch einen BTS-Stress (bias temperature gress) künstlich gealtert worden sind. Einige Gruppen der analysierten Schutzelemente sind vor der Anwendung des eigentlichen Zuverlässigkeitsstressen einem ESD-Pre-Stress unterzogen worden. Weiterhin wurde der Einfluß der Alterung des Schutzelementes durch die Anwendung eines ESD-Post-Stresses nach dem Zuverlässigkeitsstress untersucht.

Die Ergebnisse der durchgeführten Experimente werden präsentiert. Es wird weiterhin eine geeignete Freigabestrategie für Automotive-Anwendungen definiert, Mögliche Auswirkungen der Schutzelementalterung auf die finale Systemlevel-ESD-Festigkeit werden abgeleitet.
1. Introduction

ESD protection devices are part of the device pad circuitry specific to a wafer technology, which will be used in several semiconductor products. Such a device is able to transfer positive and negative electrostatic discharge pulses to ground potential faster than the device which has to be protected. The wafer technology will be qualified and released according to international standards (i.e. JEDEC JP-001, AEC-Q100/101) taking into consideration all specific reliability tests for devices, metallization and dielectrics [1-3].

But up to now there is no aligned qualification procedure existing for ESD protection devices in the valid standards to ensure the required ESD protection capability versus the required device and product lifetime. [4] describes a new qualification methodology for ESD protection devices. The procedure includes the application of ESD pulsing before and after device ageing which will be performed by dedicated device specific reliability stress tests (ESD pre- and post-stress).

For bipolar devices such reliability stress tests can be HTEO (high temperature electrical operation), BTS (bias temperature stress) or EBRB (emitter base reverse bias).

Shifts of saturation currents (e.g. in the base current of bipolar transistors), or changes of any electrical parameters like bipolar transistor base resistances due to e.g. hydrogen ions are expected after such stress tests. Furthermore, modifications of interface trap densities (e.g. at the interface between active area and the field oxide) generate variances in surface dependent breakdown voltages of specific bipolar transistor parts (e.g. between collector-base or collector-isolation).

Figure 1 shows the new qualification methodology proposal for ESD protection devices [1].

- **Stress groups**
  All qualification samples will be separated into 3 stress groups: A (reference, no reliability stress and no ESD pre-stress), B (reliability stress without ESD pre-stress) and C (reliability stress with ESD pre-stress).

- **Device package**
  All devices to be qualified will be assembled into a ceramic C-DIP (ceramic-dual-in-line-package). This package presents a standard housing of silicon chips for library device qualifications at Infineon Technologies.

- **Reliability stress tests**
  Each ESD protection device will be stressed with all necessary specific reliability stress tests.

- **ESD pre-stress**
  The samples will be pre-stressed according to HBM (human body model), standard EIA/JESD22-A114-B [5] which was used for design of the analyzed ESD protection devices. Alternatively other ESD standards can be used instead of HBM as soon as they will be used for device design. The level for ESD pre-stress is equal to the specified ESD withstanding voltage.
  The target voltage will be applied 10 times for each polarity.

- **ESD post-stress**
  The ESD post-stress is identical to the ESD pre-stress and will be applied for the stress groups B and C.
Drifts of electrical device characteristics caused by device ageing may influence the ESD robustness of the ECU (electrical control unit) on system level in particular. Therefore, the ESD post-stress is introduced. To characterize the behaviour of the ESD protection devices after pre-ageing the ESD post-stress must be applied for stress groups B and C after performing a reliability stress.

**Sample size**
A sample size of 3 wafer lots with minimum 5 devices per wafer lot and per stress group A, B and C is proposed.

During qualification the typical drift behaviour of the characteristic electrical device parameters have to be analyzed in comparison to the chosen reliability stress test drift targets.

A properly designed ESD protection device will pass the qualification if the specific drift of device parameters are not violating the defined failure criteria. These drifts must be equal for stress group B and C. Furthermore, the same conditions must be fulfilled after application of ESD post-stress to both stress groups after reliability stress test.

### 3. Test Devices

The Figure 2 shows a typical cross section of a bi-directional Zener diode which is designed as ESD protection device and used as test vehicle for the qualification procedure evaluation.

![Cross section of a typical bi-directional ESD protection Zener diode](image)

**Figure 2:** Cross section of a typical bi-directional ESD protection Zener diode

The device is characterized by a breakdown voltage in forward and backward direction. The two pn-junctions inside the device are coupled by a floating “n”-Buried Layer. The device is used in forward and reverse direction to protect the followed electrical circuit. The breakdown voltages are determined by the layout and wafer process parameters. For the investigations, ESD diodes with different breakdown voltages produced with bipolar wafer technology were used. Figure 3 shows the two typical breakdown voltages between anode and cathode of a bi-directional Zener diode on an example of a 60V-ESD diode.

![Typical breakdown voltages between anode and cathode of a bi-directional 60V-ESD diode](image)

**Figure 3:** Typical breakdown voltages between anode and cathode of a bi-directional 60V-ESD diode

Figure 4 presents a typical current characteristic between anode and cathode of a 60V-ESD diode in forward direction.

For the shown example breakdown voltages of approximately 60V for positive and negative voltages between anode and cathode were measured. A leakage current of about 0.1nA for forward voltages up to 57V can be seen.

![Typical current characteristic between anode and cathode of a 60V-ESD diode](image)

**Figure 4:** Typical current characteristic between anode and cathode of a 60V-ESD diode (forward direction)

### 4. Results of Experiments with ESD Pre-Stress

Figures 5 and 6 show the drift of the breakdown voltage (measured at a diode current of $I_D=1mA$) and the leakage current between anode and cathode of a 60V-ESD diode as a function of stress time. A BTS stress of 45V/175°C (total stress duration: 7400h) was performed for the stress groups B and C (B: no ESD pre-stress, C: ESD target pre-stress HBM, +/-4kV, 10x) according to the stress group definition in chapter 2. An ESD post-stress was not applied.

The example shows identical breakdown voltage...
drifts for stress groups B and C and no violation of drift criterion for the leakage current between anode and cathode. The device withstands an ESD pre-stress on target level of 4kV after application of reliability stress. These facts demonstrate a passed qualification.

Figure 5: Median drift of the breakdown voltage of a 60V-ESD diode after BTS 45V/175°C with/without ESD pre-stress (stress groups B/C according to Figure 1)

All measured values of leakage currents were in a range of pA. No electrical fails and no violations of drift criteria for breakdown voltage and leakage current between anode and cathode up to final stress duration of 7400h were detected during experiments. These conditions are used as release criteria for the proposed qualification procedure.

Figures 7 to 10 show typical abnormalities for a wrongly designed ESD protection diode or wafer process which were detected after first experiments according to the qualification procedure described in chapter 1. The Figure 7 displays a shifted breakdown voltage between anode and cathode after application of ESD pre-stress for a 7V-ESD diode design. The design parameters of this diode design variant are not valid to withstand the required ESD voltage target. Shown in Figure 8, due to this the leakage current between anode and cathode violates the failure criterion, too.

Figure 9 demonstrates a high breakdown voltage
shift of ~5% for a 60V-ESD diode design which was detected after the first BTS stress readout for stress group C (BTS: 60V/175°C, ESD pre-stress: HBM, +/-5kV, 10x). The half of the parameter drift criterion of 10% which has to be fulfilled after target stress duration is reached after 25h stress time. Due to the used BTS stress conditions hot carriers were moved to the interface of active area and passivation layer. A saturation effect of the device parameter is seen after the first readout, the parameter drifts afterwards until stress test end are identical for all stressed devices. Root cause for this effect is a not well-adapted passivation deposition wafer process step which built-in hot carriers and hydrogen ions into the device passivation. Different drifts of breakdown voltage between stress group B and C according to the example in Figure 10 (7V-ESD diode design, stress group B (BTS: 7V/175°C, No ESD pre-stress), stress group C (BTS: 7V/175°C, ESD pre-stress: HBM, +/-5kV, 10x) violates the defined qualification release criterion.

The small guard band between target ESD robustness and real ESD withstanding voltage for the device design caused a general weakness for withstanding the ESD pre-stress. In the following chapter experimental results of first investigations on BTS pre-aged samples of stress groups B and C including ESD post-stress are presented.

5. Results of Experiments with ESD Post-Stress

Results of the evaluation of the influence of the ESD-post-stress after performing the device ageing by BTS reliability stress are shown in Figures 11 to 16 [6]. A successful qualification run of a 7V-ESD diode design according to cross sections shown in chapter 3 is illustrated in Figures 11 to 13.

Figure 10: Different median drifts of breakdown voltage between anode and cathode of a 7V-ESD diode design for stress groups B (BTS: 7V/175°C) and C (BTS: 60V/175°C, ESD pre-stress: HBM, +/-5kV, 10x).

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(measured at a diode current $I_D=100\mu A$) no shift was detected for both stress groups related to the applied ESD post-stress (Figure 11). Furthermore, the drift of leakage current between anode and cathode is not violating the failure criterion (Figure 12). The reverse characteristic (Figure 13) presents no drift in leakage current and breakdown voltage before and after application of ESD post-stress.

11V-ESD diode after BTS 11V/175°C after a total stress duration of 7400h. For stress groups B (no ESD pre-stress) and C (ESD pre-stress: HBM, +/-4kV, 10x) an ESD post-stress (HBM, +/-4kV, 10x) was applied after the reliability test. A negative shift of the breakdown voltage (measured at a diode current $I_D=100\mu A$) after ESD post-stress for stress groups B/C is shown in Figure 14. The drift of the leakage current between anode and cathode violates the failure criterion (Figure 15). The related device reverse characteristic reflects leakage current and breakdown voltage shifts (shown in Figure 16).

Based on the presented results in Figures 14 to 16 an influence of the device ageing (due to BTS stress) on the ESD protection properties of the device after the application of ESD post-stress is given. The performed qualification was rated as failed because the ESD protection properties of the device were lost after the ESD post-stress.

To pass the qualification no variation in breakdown voltage drift and no failure criterion violation of leakage current between anode and cathode after application of ESD post-stress is allowed for stress groups B and C.

After the analysis of the experimental data on breakdown voltage and leakage current between anode and cathode a violation of the failure criteria for stress groups B and C for the 11V-ESD diode is detected (Figure 14 to 16), whereas the data for the 7V-ESD diode passed these criteria (Figures 11 to 13).

6. Conclusions

Main reasons for the different device behaviours described in chapters 4 and 5 are the design and the wafer process parameters of the investigated ESD protection device.

The device design determines the guard band between target ESD withstanding voltage and real device ESD robustness. A robust design hardens the device to be immune to deviations of wafer process parameters. A small guard band increases the probability of a failed qualification.

Wafer process parameters influence the interface properties inside the device. Especially mobile ions, interface states and oxide traps reduce the expected device life.

To release ESD protection devices for automotive power applications the drifts of devices from stress groups B and C must be identical after device specific reliability stress on the one hand. On the
other hand both stress groups must pass ESD post-stress successfully. This must be ensured by device design and wafer process capability. Infineon Technologies is using the presented procedure as qualification standard for the release of ESD protection library devices for wafer technologies in the automotive power business division. The stress duration depends on the required life time target which has to be fulfilled during qualification. The ageing of the ESD protection devices by electrical operation will influence the final ESD robustness on system level. Future activities must investigate the properties of an aged device inside a ESD protection circuitry of an ECU. A general discussion about implementation of this new device qualification procedure proposal in the standardization organizations AEC and JEDEC is necessary.

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References