

Industry Council on ESD Target Levels

Aspects of System Level ESD



Outline

- Scope and Introduction
- Field of application for component and system level ESD test
- Difference between component and system level ESD test
- Relevance of pin-specific targets
- Missing correlation between component level HBM and system level ESD
- Summary

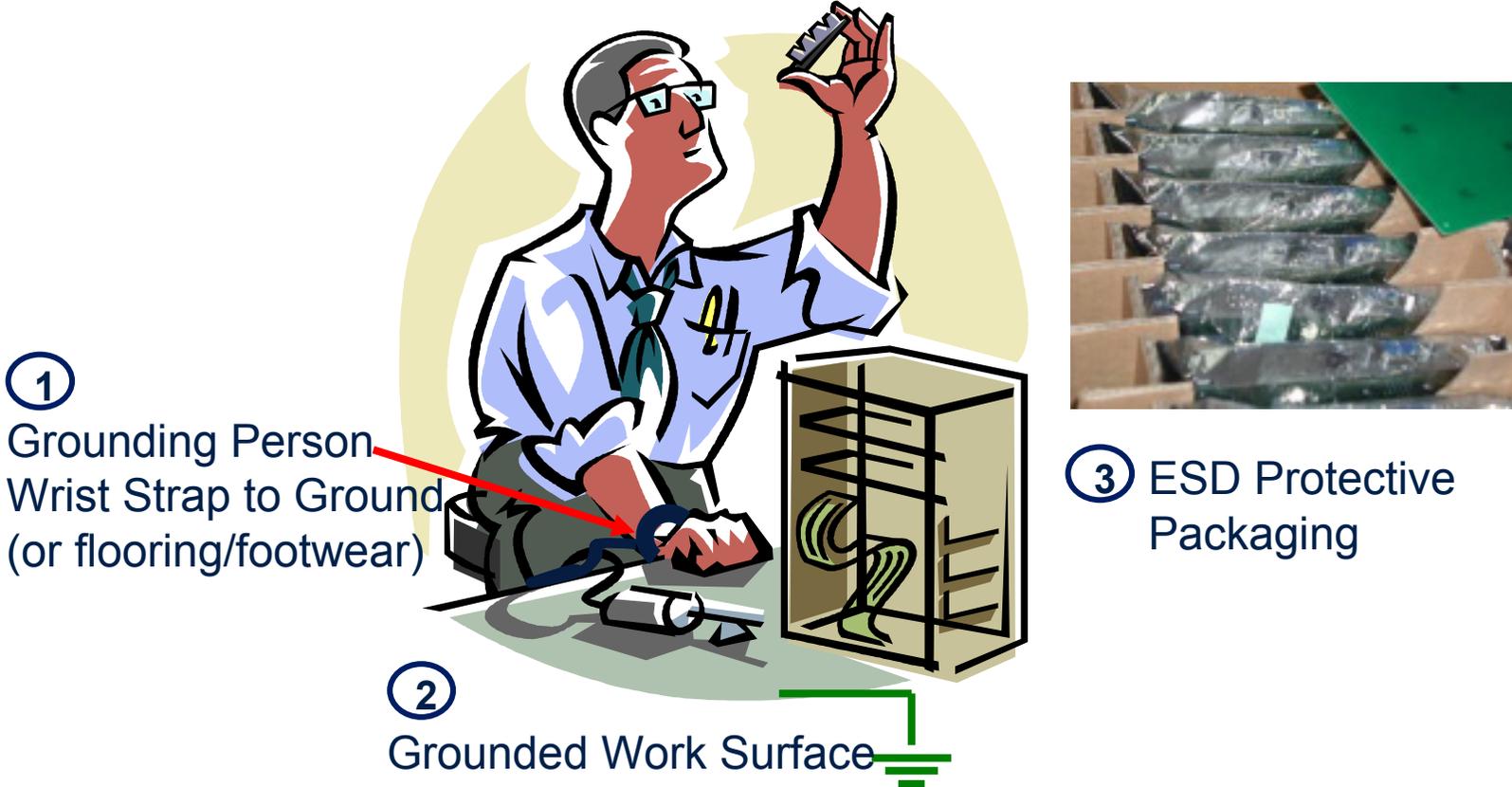
Scope

- The scope of this presentation is to describe the distinction between [Component Level ESD](#) and [System Level ESD](#), and to clarify the important but separate aspects for the ESD reliability of both models.

Introduction

- Component Level HBM/MM (according to ESDA, JEDEC or similar standards) addresses [a very different](#) ESD threat than System Level ESD tests (according to IEC)
- There is a [pervasive misunderstanding](#) that component level HBM/MM performance is critical to the system level ESD reliability
- There are challenges for designing ESD-robust systems when components will be exposed to system level ESD events such as for USB and Ethernet ports which requires a separate protection strategy
- For all cases when the IC pins are not exposed, there is [no known link](#) between the two models

ESD Field Events During Manufacturing in an ESD Protected Area



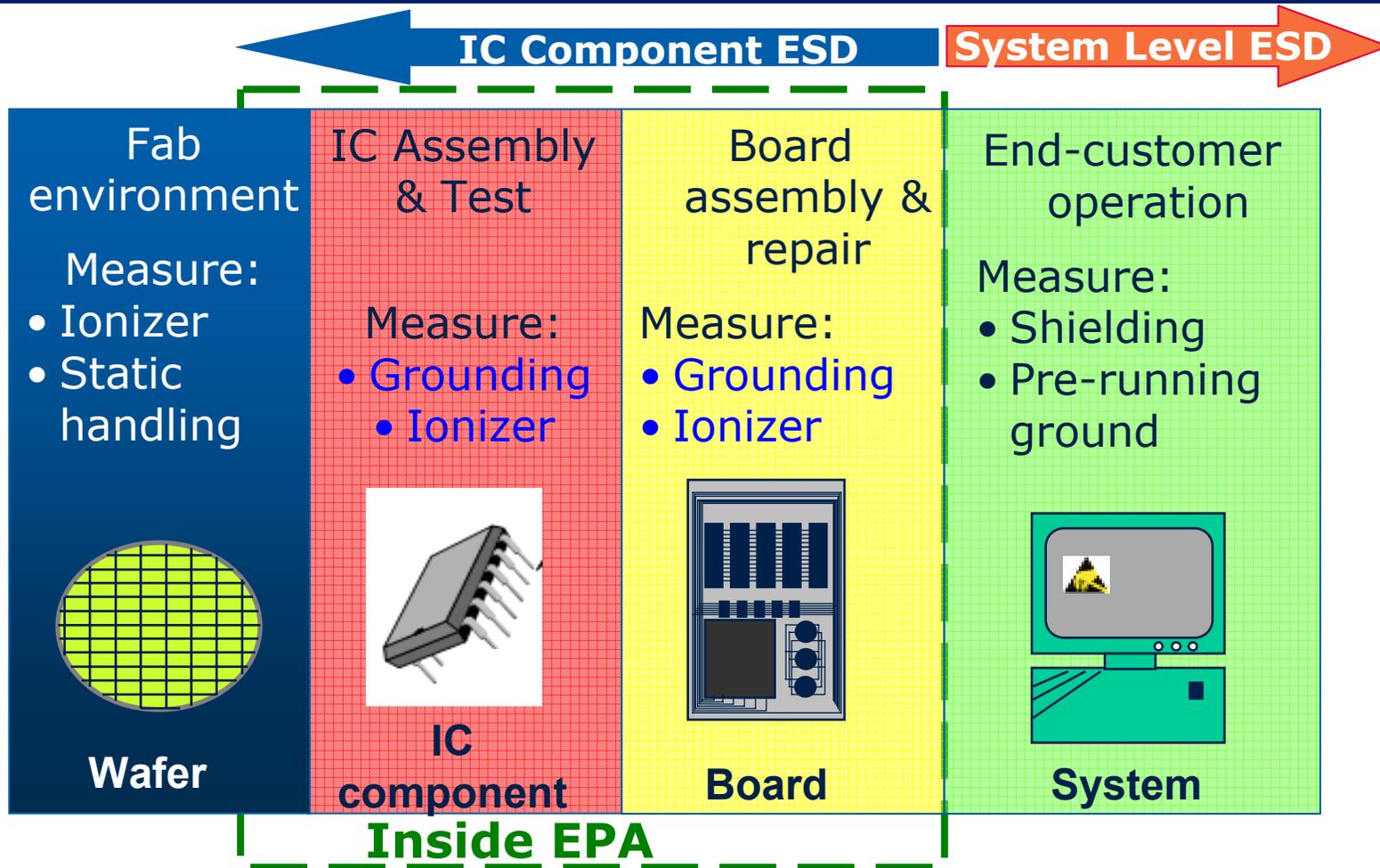
Addressed by component level ESD testing

ESD Field Events on System Level occur in an unprotected area

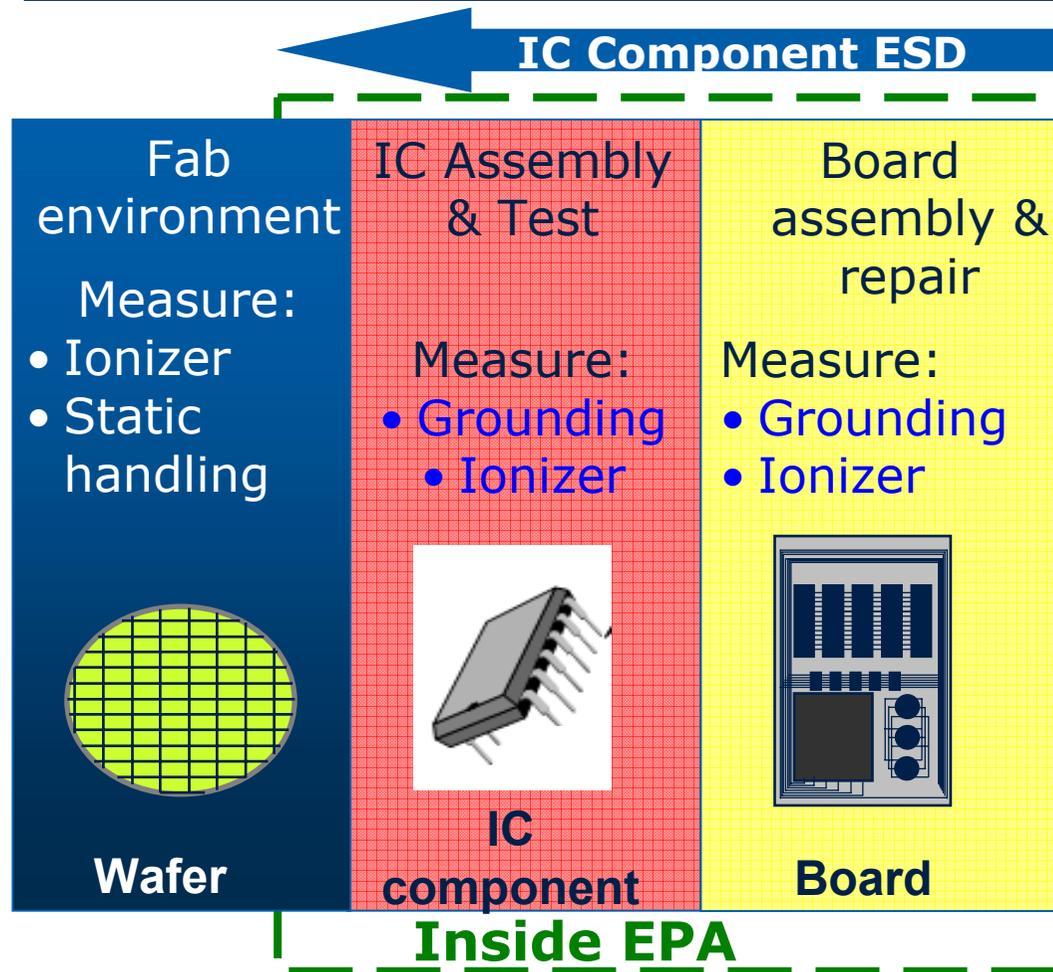


Discharges from a handheld metallic tool to a system (outside an EPA) are tested by system level ESD (e.g. IEC 61000-4-2)

Stages of ESD Models and Protection Methods/Design



Inside ESD Protected Area (EPA) - ESD Protection Methods and Design



- Well controlled environment (EPA) required
- On-chip ESD protection compliant with several hundred Volts HBM guarantees safe handling
- Protection realized between any pin combination
- Covers from backend manufacturing (BEOL) to board mounting

Outside EPA - Protection Methods and Design

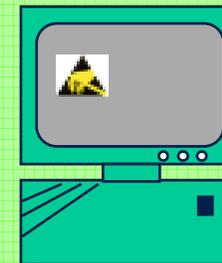
- System level ESD protection necessary to satisfy higher ESD levels
- ESD Packaging can protect boards outside EPA
- Enhanced protection design applies only to the very few exposed pins
- Covers from board handling to end-user operation
- Component level ESD protection design for the non-exposed pins does not influence system level ESD robustness

System Level ESD

End-customer operation

Measure:

- Shielding
- Pre-running ground

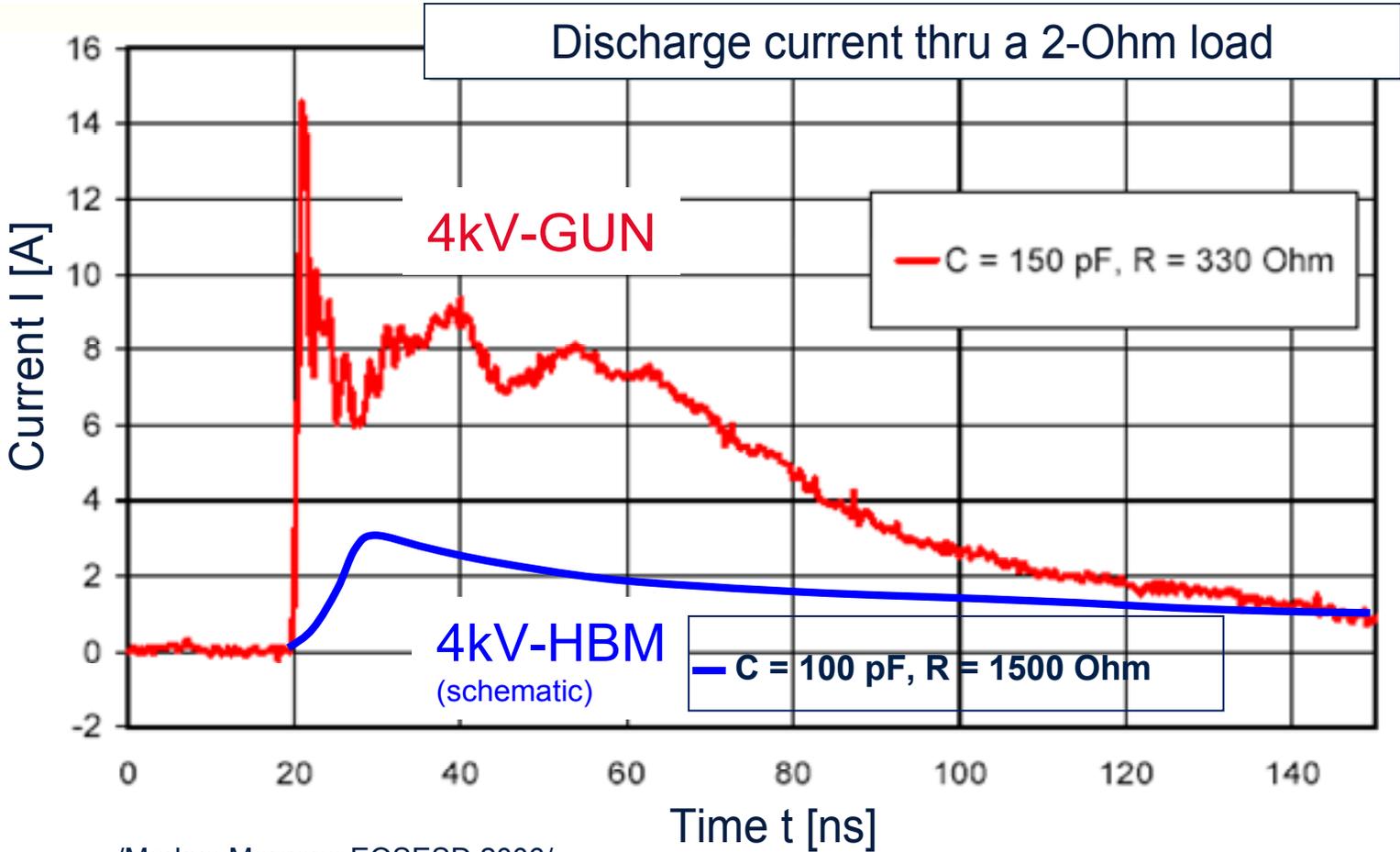


System

Comparison of Component and System Level ESD Stress

Function	Device level ESD test	System level ESD Test (IEC)
Stressed pin group	All pin combinations	Few special pins
Supply	Unpowered	Powered & unpowered
Test methodology	Standardized	Application specific
Test set-up	Commercial tester & sockets	Application specific
Typical qualification goal	1 ...2 kV JEDEC HBM	8 kV Contact (IEC 61000-4-2) 15kV Air (IEC 61000-4-2)
Corresponding peak current	0.65 ... 1.3 A	> 20 A
Failure signature	Destructive	Functional or destructive

Waveform of Component HBM and System Level Gun Test

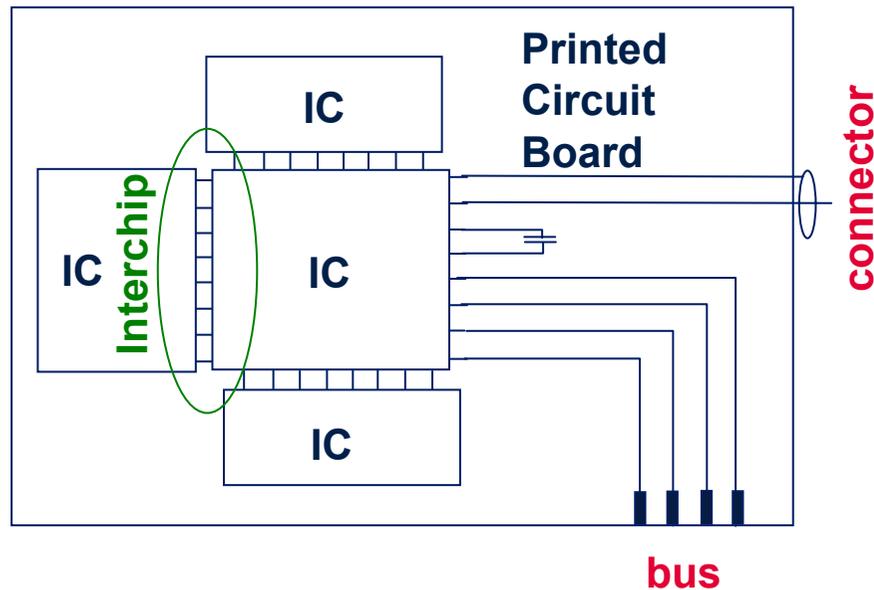


/Markus Mergens EOESD 2006/

System Level ESD Stress of Powered Systems

- System level ESD gun test has also to be performed under powered conditions
- For powered systems there are two failure mechanisms
 - Destructive fail
 - Functional fail
- The primary destructive fail does not typically dominate due to the sinking of the pulse current to supply sources
- The functional fail (e.g. latch-up) is most common and cannot be addressed by classical ESD protection methods
- There is no correlation with HBM robustness.

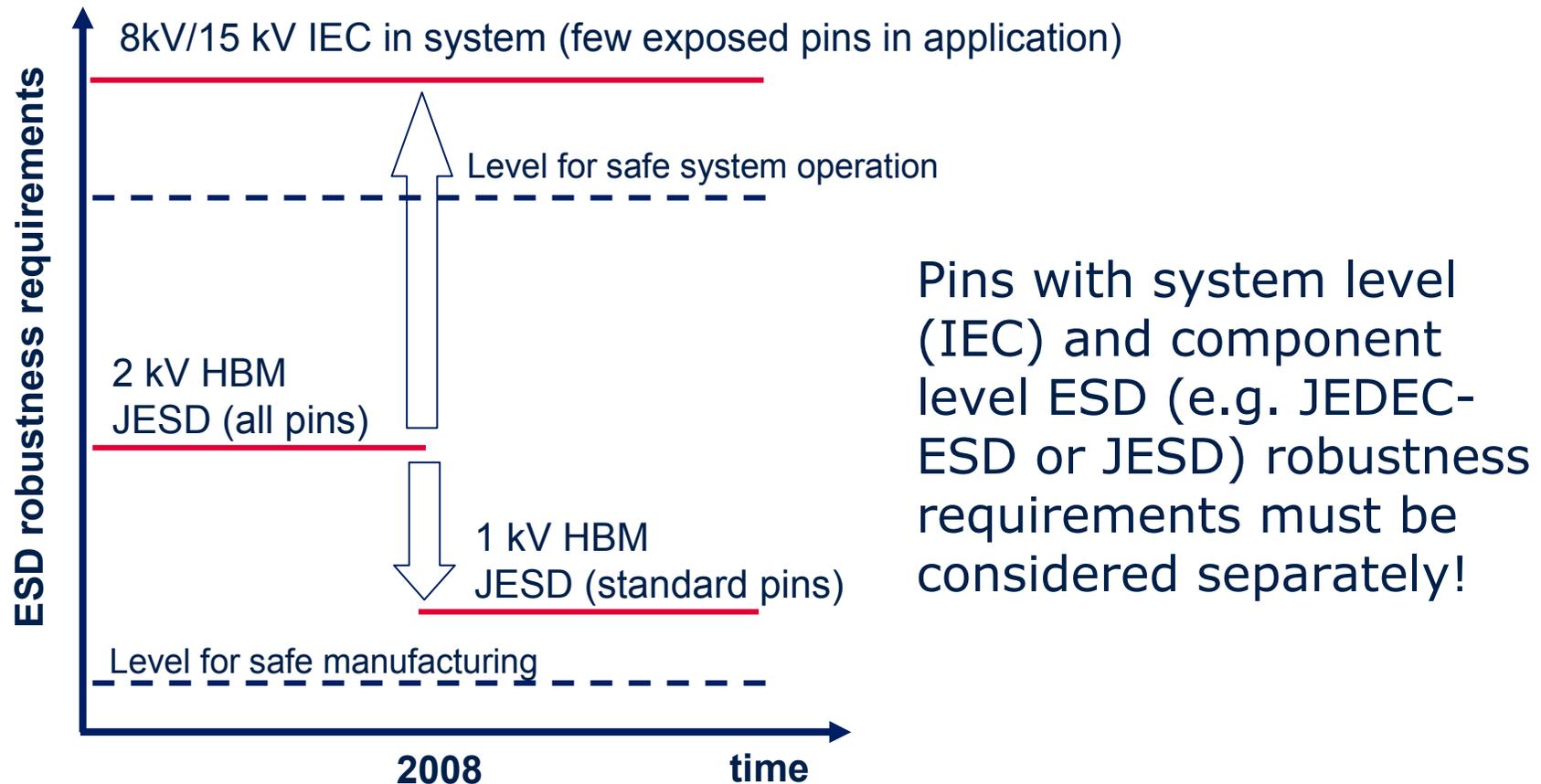
Classes of Pins with Specific System Level ESD Robustness



Pin types:

- On board interchip connection
→ **non-critical** pins for system level ESD
- Pins attached to signal busses (e.g. CAN) connecting several PCBs (exposed pin during repair)
→ **critical** pins for system level ESD
- Pins attached to external connectors (e.g. exposed USB pins)
→ **critical** pins for system level ESD

Appropriate Choice of Pin Specific ESD Robustness Level



Missing correlation between Component and System level ESD robustness

Example #1

- One IC processed in 0.35 μm technology passed 1.5kV HBM at first silicon
- The device was tested for its IEC performance in the system board
- The required IEC 61000-4-2 level was achieved on pins exhibiting 1.5kV HBM
- A redesign effort was made to improve the device HBM performance
- After the redesign, the same pins showed an improved 2kV HBM level in the component level testing
- But the “improved” device failed the previously passed IEC level test

→ Improving component level performance has no correlation to its IEC level performance in a system board

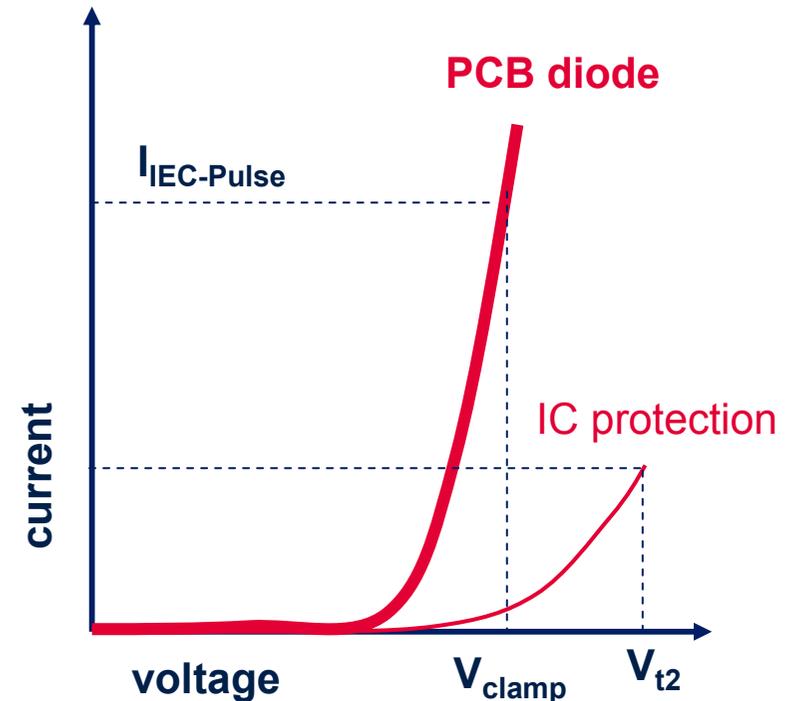
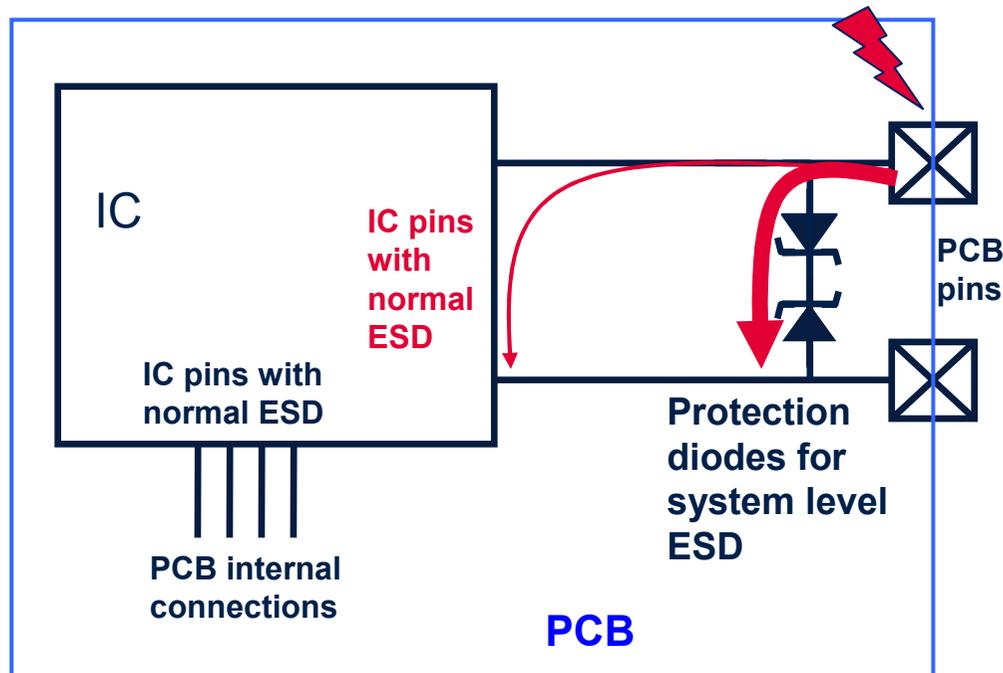
Missing correlation between Component and System level ESD robustness

Example #2

- Several IC products built in 90nm CMOS technology met only 500V HBM on several pins
- There were no component level ESD failures for any of these shipped products into the millions
- These were placed in different customer system board applications and were tested with the IEC stress as required by the individual customers
- All devices passed 2kV or 4kV or 8kV IEC tests by the different customers

→ Low HBM performance for safely shipped products have no correlation to the system level tests

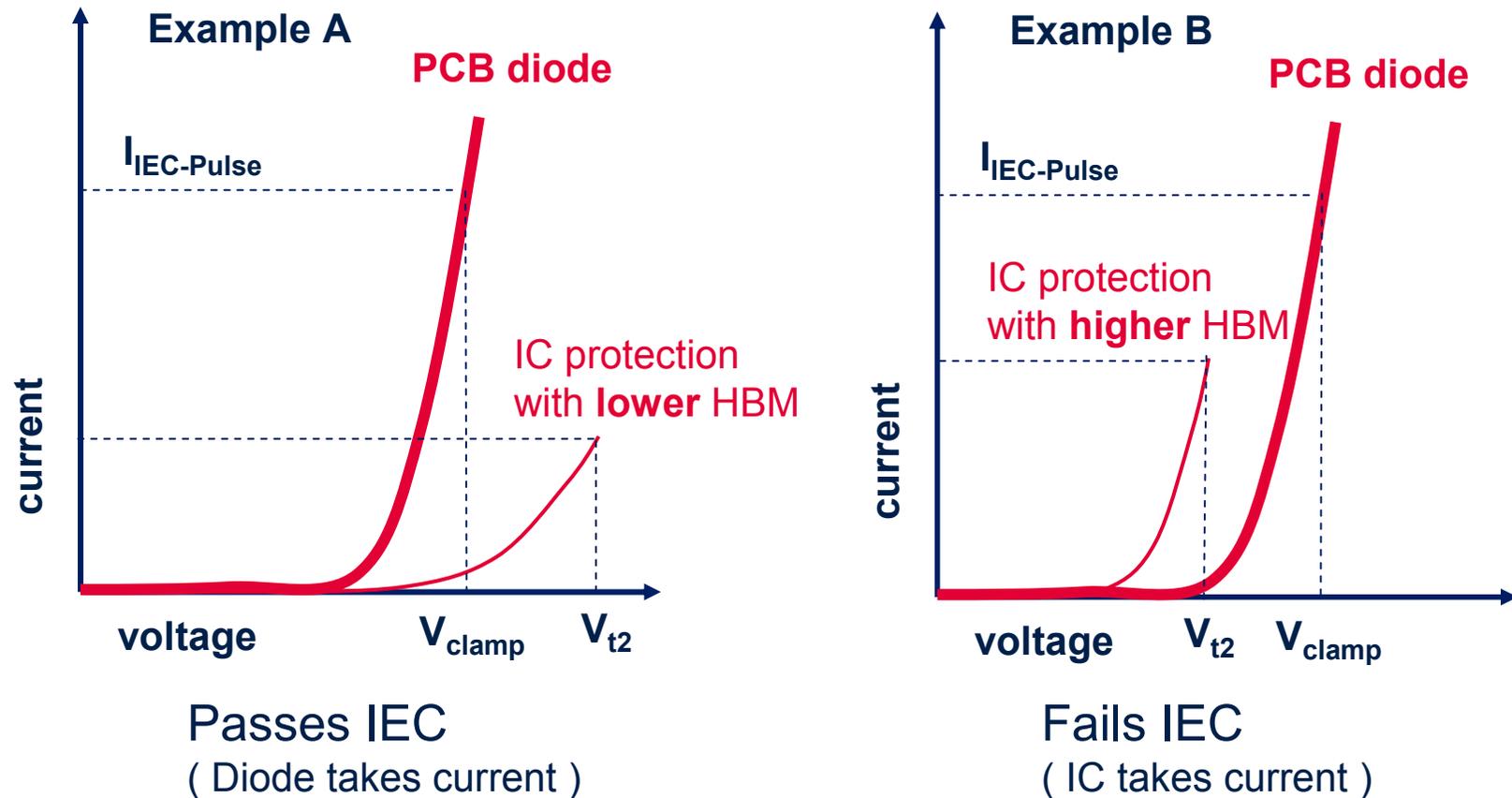
Strategy for System Level ESD Protection (1)



Common strategy with PCB protection (co-design approach) is to shunt most of the current by the PCB diode

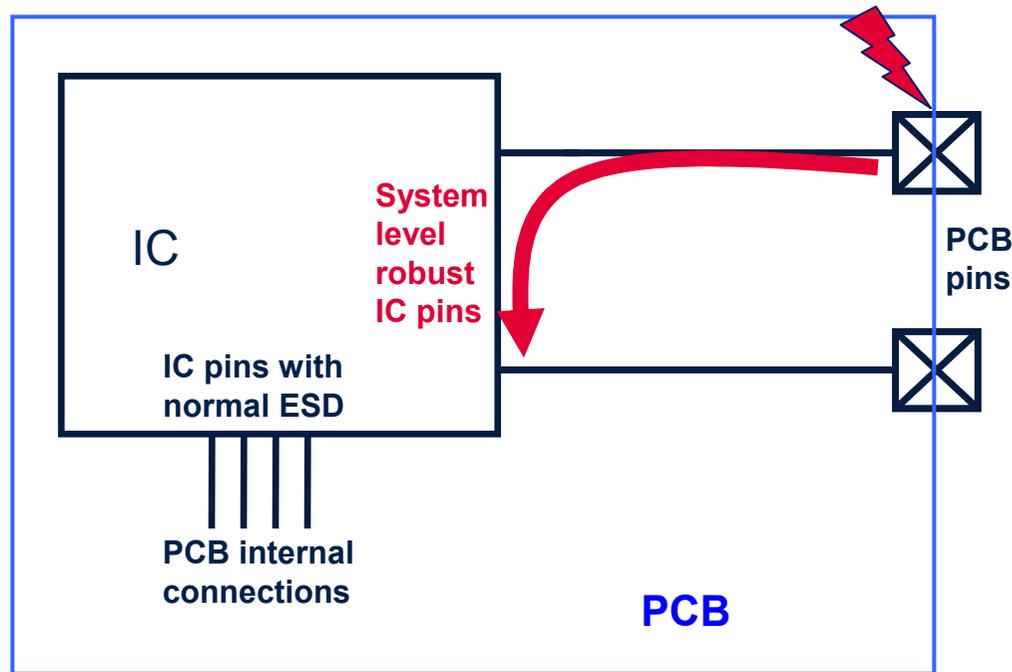
Design goal :
Failing voltage of IC $V_{t2} > V_{clamp}$

Pitfall in Correlating HBM Level to IEC Robustness



Higher HBM level is no indication for a sufficient failure voltage V_{t2}

Strategy for system level ESD protection (2)



Inherently robust IC pins
(on-chip protection far beyond 2 kV HBM)

- High IEC pulse current leads to an increase of on-chip area of protection element by a factor of 10
- Increased pad capacitance degrades high speed performance
- Both concepts (inherent & co-design) need to be evaluated under economical and technical aspects case by case

Conclusions on Missing Correlation

- Component Level HBM/MM (according to ESDA, JEDEC or similar standards) addresses a very different field situation than System Level ESD tests (according to IEC)
- Higher HBM/MM robustness does not guarantee high system level ESD robustness
- Lower HBM/MM does not on the other hand result in system failures

Summary

- Minimum component level ESD is always required for safe handling in ESD Protected Areas (EPA)
- With the required controls in EPA, high levels of component level ESD are not necessary
- Component level ESD is not directly coupled to system level ESD
- System level ESD requires its own protection design methods and needs to be characterized by appropriate methods (see ongoing work at IEC TS 62228, ESDA WG 5.6 and application-specific approaches)
- Therefore, lowering the component level ESD to a safe required value does not degrade yield in manufacturing chain nor reliability at the end-user
- Lowering component ESD requirements does not compromise system level ESD performance

Backup

Parameters and Pitfalls of Robust System Level ESD Design

- System level stress directly on device can result in different failure mode
- On board ESD protective elements are usually necessary
- Implementing board level protection circuits requires IC/PCB co-design
- System level ESD robustness is dependent on wiring/ circuits on board
- System level robustness also depends on system level packaging (shielding, surge suppressors, connector design, etc.)